IN THE CLAIMS

Please amend claims 1-6 and 8-25 as follows:

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1. (currently amended) A method of ~~reproducing~~ replacing a mark on a semiconductor wafer, ~~wherein, in a case where a predetermined~~the mark replacing an original mark that~~which~~ has been ~~made on a semiconductor wafer beforehand during the course of manufacture or processing is substantially~~at least partially ~~effaced in association with progress of~~during manufacturing or processing subsequent to placing the original~~operation, a mark essentially identical with the substantially effaced mark is formed at another location spaced apart from the substantially effaced~~ mark, comprising steps of:

forming a second mark on the wafer, identical to the first mark, in a second location of the wafer, spaced apart from the first location.

2. (currently amended) A method of ~~reproducing~~ replacing a mark on a semiconductor wafer, ~~wherein, in a case where any one of predetermined single essentially~~ having identical marks ~~which have been made~~ in two or more first locations, the mark replacing at least one original mark that has been at least partially effaced during ~~on a semiconductor wafer beforehand during the course of manufacture~~manufacturing or processing ~~is substantially effaced in association with progress of manufacturing operation or processing operation, a mark essentially identical with the substantially effaced mark is reproduced by reference to the substantially remaining other marks~~subsequent to placing the original marks, comprising the steps of:

forming a mark identical to the at least one original partially-effaced mark by reference to the remaining mark.

3. (currently amended) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the at least ~~substantially~~partially-effaced mark is reproduced by

means of forming a mark ~~essentially identical with~~similar to the ~~substantially~~partially-effaced mark at another second location spaced apart from the ~~substantially~~partially-effaced mark.

4. (currently amended) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the ~~substantially~~partially-effaced mark is reproduced by means of forming a mark ~~essentially identical with~~similar to the ~~substantially~~partially-effaced mark at another second location in the vicinity of the ~~substantially~~partially-effaced mark.

5. (currently amended) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and the ~~substantially~~partially-effaced mark is reproduced by means of forming a mark ~~essentially identical with~~similar to the ~~substantially~~partially-effaced mark at another second location in the vicinity of the ~~substantially~~partially-effaced mark.

6. (currently amended) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is a minute ID mark which is assigned to the semiconductor wafer and is formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and the ~~substantially~~partially-effaced mark is reproduced by means of forming a mark ~~essentially identical with~~similar to the ~~substantially~~partially-effaced mark at another second location in the vicinity of the ~~substantially~~partially-effaced mark.

7. (original) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is a mark affixed on the interior wall surface of a notch.

8. (currently amended) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is a mark affixed on the interior wall surface of a notch, and the ~~substantially~~partially-effaced mark is reproduced by means of

forming a mark ~~essentially identical with~~similar to the ~~substantially~~partially-effaced mark at another second location spaced apart from the ~~substantially~~partially-effaced mark.

9. (currently amended) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is a mark affixed on the interior wall surface of a notch, and the ~~substantially~~partially-effaced mark is reproduced by means of forming a mark ~~essentially identical with~~similar to the ~~substantially~~partially-effaced mark at another second location in the vicinity of the ~~substantially~~partially-effaced mark.

10. (currently amended) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is formed by means of a combination of dots, each dot measuring 1 to 13 μm wide and is affixed on the interior wall surface of a notch, and the ~~substantially~~partially-effaced mark is reproduced by means of forming a mark ~~essentially identical with~~similar to the ~~substantially~~partially-effaced mark at another second location in the vicinity of the ~~substantially~~partially-effaced mark.

11. (currently amended) The method of reproducing a mark on a semiconductor wafer according to claim 2, wherein the predetermined mark is an ID mark which is assigned to the semiconductor wafer, is formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and is affixed on the interior wall surface of a notch, and the ~~substantially~~partially-effaced mark is reproduced by means of forming a mark ~~essentially identical with~~similar to the ~~substantially~~partially-effaced mark at another second location in the vicinity of the ~~substantially~~partially-effaced mark.

12. (currently amended) A semiconductor wafer for distribution purpose having two or more ~~essentially identical~~similar marks formed thereon.

13. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein two or more ~~essentially identical~~similar marks are provided at positions where

the marks are to undergo the same surface treatment at different speeds during the course of manufacture.

14. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture.

15. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks are located close to each other and such that the marks undergo the same surface treatment at different speeds during the course of manufacture.

16. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

17. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein two or more ~~essentially identical~~similar marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture

and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

18. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein two or more ~~essentially identical~~similar marks are minute ID marks which are assigned to the semiconductor wafer and are formed by means of a combination of dots, each dot measuring 1 to 13 μm wide, and some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

19. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein two or more ~~essentially identical~~similar marks are minute ID marks which are assigned to the semiconductor wafer, are formed by means of a combination of dots, each dot measuring 1 to 13 μm, and are affixed on the interior wall surface of a notch, and some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

20. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein two or more ~~essentially identical~~similar marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm for positioning purpose, and some of two or more ~~essentially identical~~ similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the

course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

21. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein two or more ~~essentially identical~~similar marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm and indicate crystal orientation of the semiconductor wafer, and some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

22. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein the semiconductor wafer is perfectly annular; two or more ~~essentially identical~~similar marks are formed by means of a combination of dots, each dot measuring 1 to 13 μm and indicate crystal orientation of the semiconductor wafer; and some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

23. (currently amended) The semiconductor wafer for distribution purpose according to claim 12, wherein two or more ~~essentially identical~~similar marks are aligned in a single direction; and some of two or more ~~essentially identical~~similar marks are provided on the front side of the semiconductor wafer and the other ~~essentially identical~~similar marks are provided on the reverse side of the same, such that the marks undergo the same surface treatment at different speeds during the course of manufacture and such that the marks are located within an area where a single optical reading machine can read the marks simultaneously.

24. (currently amended) Use of a semiconductor wafer on which two or more ~~essentially identical~~similar marks are formed by means of marking the semiconductor wafer during the course of manufacture or processing.

25. (currently amended) A method of obviating a demerit, which would otherwise be caused when a single mark is ~~substantially~~ effaced in association with manufacture or processing of a semiconductor wafer, by means of marking a semiconductor wafer with two or more ~~essentially identical~~similar marks during the course of manufacture or processing.